7.3.1.3 Detailed Command Description

The following table provides a detailed description of the SPI bus commands. The responses are defined in Section 7.3.2. Table 7-3 lists all SD Memory Card commands. A "yes" in the SPI mode column indicates that the command is supported in SPI mode. With these restrictions, the command class description in the CSD is still valid. If a command does not require an argument, the value of this field should be set to zero. The reserved commands are reserved in SD mode as well.

The binary code of a command is defined by the mnemonic symbol. As an example, the content of the **command index** field is (binary) '000000' for CMD0 and '100111' for CMD39.

The card shall ignore stuff bits and reserved bits in an argument.

CMD INDEX	SPI Mode	Argument	Resp	Abbreviation	Command Description
CMD0	Yes	[31:0] stuff bits	R1	GO_IDLE_STATE	Resets the SD Memory Card
CMD1	Yes[1]	[31]Reserved bit [30]HCS [29:0]Reserved bits	R1	SEND_OP_ COND	Sends host capacity support information and activates the card's initialization process. HCS is effective when card receives SEND_IF_COND command. Reserved bits shall be set to '0'.
CMD2	No				
CMD3	No				
CMD4	No				
CMD5	Reserved for I/O Mode (refer to the "SDIO Card Specification")				
CMD6[8]	Yes	[31] Mode 0:Check function 1:Switch function [30:24] reserved (All '0') [23:20] reserved for function group 6 (All '0' or 0xF) [19:16] reserved for function group 5 (All '0' or 0xF) [15:12] reserved for function group 4 (All '0' or 0xF) [11:8] reserved for function group 3 (All '0' or 0xF) [7:4] function group 2 for command system [3:0] function group 1 for access mode	R1	SWITCH_FUNC	Checks switchable function (mode 0) and switches card function (mode 1). See Section 4.3.10.
CMD7	No				

CMD INDEX	SPI Mode	Argument	Resp	Abbreviation	Command Description
CMD8[9]	Yes	[31:12]Reserved bits [11:8]supply voltage(VHS) [7:0]check pattern	R7	SEND_IF_COND	Sends SD Memory Card interface condition that includes host supply voltage information and asks the accessed card whether card can operate in supplied voltage range. Reserved bits shall be set to '0'.
CMD9	Yes	[31:0] stuff bits	R1	SEND_CSD	Asks the selected card to send its card-specific data (CSD)
CMD10	Yes	[31:0] stuff bits	R1	SEND_CID	Asks the selected card to send its card identification (CID)
CMD11	No				
CMD12	Yes	[31:0] stuff bits	R1b[5]	STOP_ TRANSMISSION	Forces the card to stop transmission in Multiple Block Read Operation
CMD13	Yes	[31:0] stuff bits	R2	SEND_STATUS	Asks the selected card to send its status register.
CMD14	reserved				
CMD15	No				
CMD16	Yes	[31:0] block length	R1	SET_BLOCKLEN	In case of SDSC Card, block length is set by this command. In case of SDHC and SDXC Cards, block length of the memory access commands are fixed to 512 bytes. The length of LOCK_UNLOCK command is set by this command regardless of card capacity.
CMD17	Yes	[31:0] data address[10]	R1	READ_SINGLE_ BLOCK	Reads a block of the size selected by the SET_BLOCKLEN command.[3]
CMD18	Yes	[31:0] data address[10]	R1	READ_MULTIPL E_BLOCK	Continuously transfers data blocks from card to host until interrupted by a STOP_TRANSMISSION command.
CMD19	reserved				
CMD20	No				
CMD21... CMD23	reserved				
CMD24	Yes	[31:0] data address[10]	R1	WRITE_BLOCK	Writes a block of the size selected by the SET_BLOCKLEN command.[4]
CMD25	Yes	[31:0] data address[10]	R1	WRITE_MULTIPL E_BLOCK	Continuously writes blocks of data until 'Stop Tran' token is sent (instead 'Start Block').
CMD26	No				
CMD27	Yes	[31:0] stuff bits	R1	PROGRAM_CSD	Programming of the programmable bits of the CSD.

CMD INDEX	SPI Mode	Argument	Resp	Abbreviation	Command Description
CMD28	Yes	[31:0] data address	R1b[5]	SET_WRITE_ PROT	If the card has write protection features, this command sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE). SDHC and SDXC Cards do not support this command.
CMD29	Yes	[31:0] data address	R1b[5]	CLR_WRITE_ PROT	If the card has write protection features, this command clears the write protection bit of the addressed group. SDHC and SDXC Cards do not support this command.
CMD30	Yes	[31:0] write protect data address	R1	SEND_WRITE_ PROT	If the card has write protection features, this command asks the card to send the status of the write protection bits.[6] SDHC and SDXC Cards do not support this command.
CMD31	reserved				
CMD32	Yes	[31:0] data address[10]	R1	ERASE_WR_BL K_START_ADDR	Sets the address of the first write block to be erased.
CMD33	Yes	[31:0] data address[10]	R1	ERASE_WR_BL K_END_ADDR	Sets the address of the last write block of the continuous range to be erased.
CMD34-37[8]	Reserved for each command system set by switch function command (CMD6). Refer to each command system specification for more detail.				
CMD38	Yes	[31:0] stuff bits	R1b[5]	ERASE	Erases all previously selected write blocks. FULE and DISCARD are not supported through SPI interface.
CMD39	No				
CMD40	No				
CMD41	Reserved				
CMD42	Yes	[31:0] Reserved bits (Set all 0)	R1	LOCK_UNLOCK	Used to Set/Reset the Password or lock/unlock the card. A transferred data block includes all the command details - refer to Section 0. The size of the Data Block is defined with SET_BLOCK_LEN command. Reserved bits in the argument and in Lock Card Data Structure shall be set to 0.
CMD43-49 CMD51	reserved				
CMD50[8]	Reserved for each command system set by switch function command (CMD6). Refer to each command system specification for more detail.				
CMD52-54	Reserved for I/O Mode (refer to the "SDIO Card Specification")				

CMD INDEX	SPI Mode	Argument	Resp	Abbreviation	Command Description
CMD55	Yes	[31:0] stuff bits	R1	APP_CMD	Defines to the card that the next command is an application specific command rather than a standard command
CMD56	Yes	[31:1] stuff bits. [0]: RD/WR[7]	R1	GEN_CMD	Used either to transfer a Data Block to the card or to get a Data Block from the card for general purpose/application specific commands. In case of Standard Capacity SD Memory Card, the size of the Data Block shall be defined with SET_BLOCK_LEN command. In case of SDHC and SDXC Cards, block length of this command is fixed to 512-byte.
CMD57[8]	Reserved for each command system set by switch function command (CMD6). Refer to each command system specification for more detail.				
CMD58	Yes	[31:0] stuff bits	R3	READ_OCR	Reads the OCR register of a card. CCS bit is assigned to OCR[30].
CMD59	Yes	[31:1] stuff bits [0:0] CRC option	R1	CRC_ON_OFF	Turns the CRC option on or off. A '1' in the CRC option bit will turn the option on, a '0' will turn it off
CMD60-63	Reserved For Manufacturer				

1. CMD1 is valid command for the Thin (1.4mm) Standard Size SD Memory Card only if used after re-initializing a card (not after power on reset).
2. The default block length is as specified in the CSD.
3. The data transferred shall not cross a physical block boundary unless READ_BLK_MISALIGN is set in the CSD.
4. The data transferred shall not cross a physical block boundary unless WRITE_BLK_MISALIGN is set in the CSD.
5. R1b: R1 response with an optional trailing busy signal
6. 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data line. The last (least significant) bit of the protection bits corresponds to the first addressed group. If the addresses of the last groups are outside the valid range, then the corresponding write protection bits shall be set to zero
7. RD/WR_: "1" the Host shall get a block of data from the card.
   "0" the host sends block of data to the card.
8. This command was added in spec version 1.10
9. This command is added in spec version 2.00
10. SDSC Card (CCS=0) uses byte unit address and SDHC and SDXC Cards (CCS=1) use block unit address (512 bytes unit).

Table 7-3 : Commands and Arguments

The following table describes all the application specific commands supported/reserved by the SD Memory Card. All the following commands shall be preceded with APP_CMD (CMD55).

CMD INDEX	SPI Mode	Argument	Resp	Abbreviation	Command Description
ACMD6	No				
ACMD13	yes	[31:0] stuff bits	R2	SD_STATUS	Send the SD Status. The status fields are given in Table 4-44
ACMD17	reserved				
ACMD18	yes	--	--	--	Reserved for SD security applications1
ACMD19-ACMD21	reserved				
ACMD22	yes	[31:0] stuff bits	R1	SEND_NUM_WR_BLOCKS	Send the numbers of the well written (without errors) blocks. Responds with 32-bit+CRC data block.
ACMD23	yes	[31:23] stuff bits [22:0]Number of blocks	R1	SET_WR_BLK_ERASE_COUNT	Set the number of write blocks to be pre-erased before writing (to be used for faster Multiple Block WR command). "1"=default (one wr block)(2).
ACMD24	reserved				
ACMD25	yes	--	--	--	Reserved for SD security applications[1]
ACMD26	yes	--	--	--	Reserved for SD security applications[1]
ACMD38	yes	--	--	--	Reserved for SD security applications[1]
ACMD39 - ACMD40	reserved				
ACMD41	Yes	[31]Reserved bit [30]HCS [29:0]Reserved bits	R1	SD_SEND_OP_COND	Sends host capacity support information and activates the card's initialization process. Reserved bits shall be set to '0'
ACMD42	yes	[31:1] stuff bits [0]set_cd	R1	SET_CLR_CARD_DETECT	Connect[1]/Disconnect[0] the 50 KOhm pull-up resistor on CS (pin 1) of the card. The pull-up may be used for card detection.
ACMD43-ACMD49	yes	--	--	--	Reserved for SD security applications[1]
ACMD51	yes	[31:0] stuff bits	R1	SEND_SCR	Reads the SD Configuration Register (SCR).

(1) Refer to the "Part3 Security Specification" for detailed explanation about the SD Security Features
(2) Stop Tran Token shall be used to stop the transmission in Write Multiple Block whether the pre-erase (ACMD23) feature is used or not.

Table 7-4 : Application Specific Commands used/reserved by SD Memory Card - SPI Mode

7.3.1.4 Card Operation for CMD8 in SPI mode

In SPI mode, the card always returns response. Table 7-5 shows the card operation for CMD8.

Command Argument Check					Response of Card *1			
Index	**Reserved**	**VHS**	**Pattern**	**CRC**	**R1**	**Reserved**	**VCA**	**Pattern**
=8	Don't Care	Don't Care	Don't Care	Error	09h	(R1 only)		
Not 8	Don't Care	Don't Care	Don't Care	Don't Care	Depends on command index			
=8	Don't Care	Mismatch *2	Don't Care	Correct	01h	0	0	Echo Back
=8	Don't Care	Match *2	Don't Care	Correct	01h	0	Echo Back	Echo Back

*1: Response indicates the actual response that the card returns. (It does not include errors during transfer response.)
*2: 'Match' means AND of following condition a) and b). 'Mismatch' is other cases.
a) Only 1 bit is set to '1' in VHS.
b) The card supports the host supply voltage.

Table 7-5 : Card Operation for CMD8 in SPI Mode

7.3.2 Responses

There are several types of response tokens. As in SD mode, all are transmitted MSB first.
Multiple bytes responses are defined in SPI mode but the card outputs only first byte (equivalent to R1) when Illegal Command Error or Command CRC Error is indicated in it. In this case, host never reads as the multiple bytes of response.

7.3.2.1 Format R1

This response token is sent by the card after every command with the exception of SEND_STATUS commands. It is one byte long, and the MSB is always set to zero. The other bits are error indications, an error being signaled by a 1. The structure of the R1 format is given in Figure 7-9. The meaning of the flags is defined as following:

In idle state: The card is in idle state and running the initializing process.
Erase reset: An erase sequence was cleared before executing because an out of erase sequence command was received.
Illegal command: An illegal command code was detected.
Communication CRC error: The CRC check of the last command failed.
Erase sequence error: An error in the sequence of erase commands occurred.
Address error: A misaligned address that did not match the block length was used in the command.
Parameter error: The command's argument (e.g. address, block length) was outside the allowed range for this card.

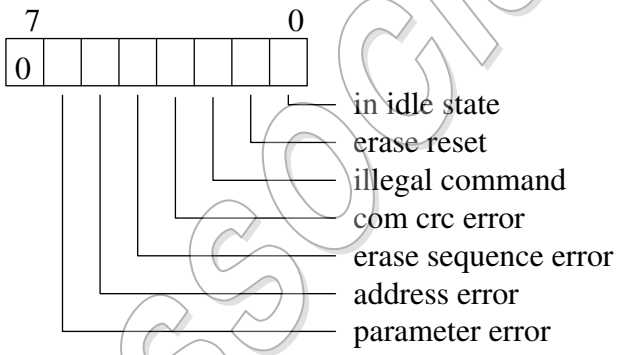

Figure 7-9 : R1 Response Format

7.3.2.2 Format R1b

This response token is identical to the R1 format with the optional addition of the busy signal. The busy signal token can be any number of bytes. A zero value indicates card is busy. A non-zero value indicates the card is ready for the next command.

7.3.2.3 Format R2

This response token is two bytes long and sent as a response to the SEND_STATUS command. The format is given in Figure 7-10.

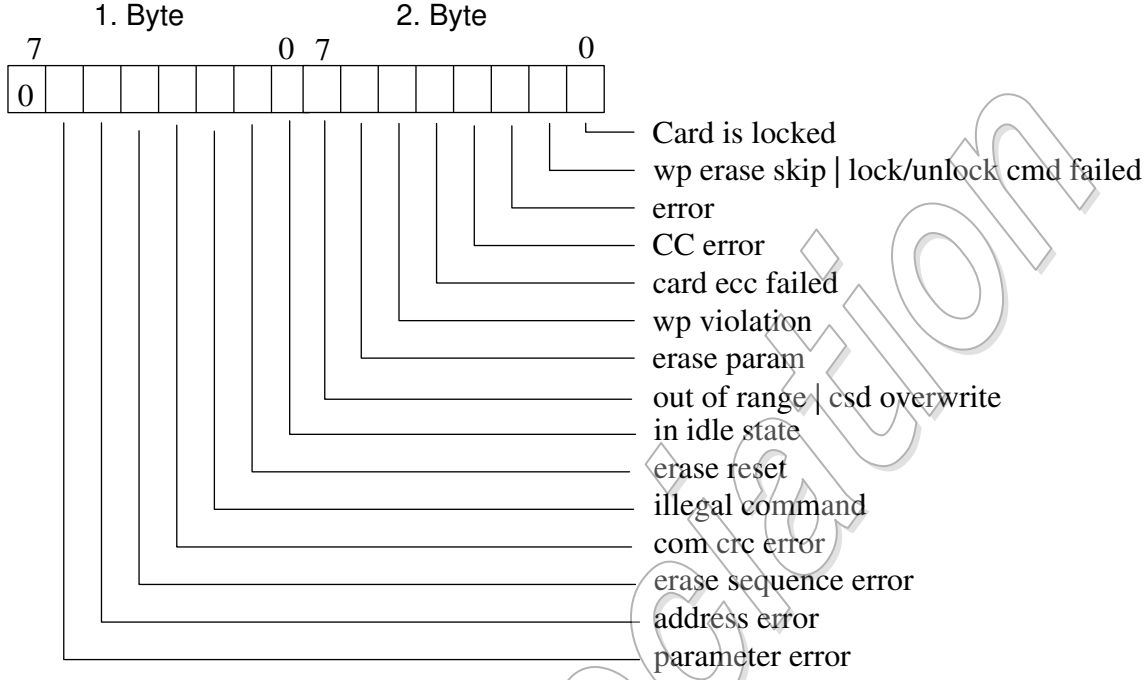

Figure 7-10 : R2 Response Format

The first byte is identical to the response R1. The content of the second byte is described in the following:

Erase param: An invalid selection for erase, sectors or groups.
Write protect violation: The command tried to write a write-protected block.
Card ECC failed: Card internal ECC was applied but failed to correct the data.
CC error: Internal card controller error.
Error: A general or an unknown error occurred during the operation.
Write protect erase skip | lock/unlock command failed:
This status bit has two functions overloaded. It is set when the host attempts to erase a write-protected sector or makes a sequence or password errors during card lock/unlock operation.
Card is locked: Set when the card is locked by the user. Reset when it is unlocked.

7.3.2.4 Format R3

This response token is sent by the card when a READ_OCR command is received. The response length is 5 bytes (see Figure 7-11). The structure of the first (MSB) byte is identical to response type R1. The other four bytes contain the OCR register.

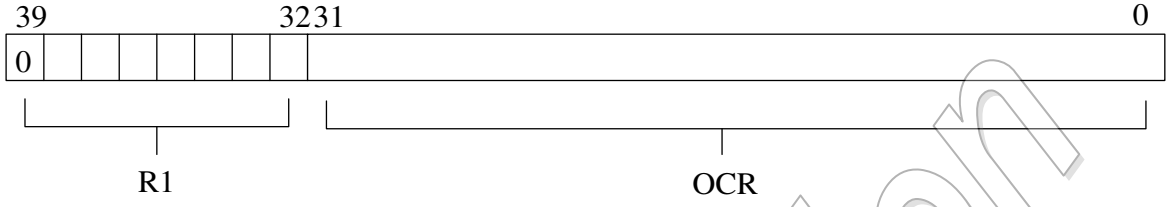

Figure 7-11 : R3 Response Format

7.3.2.5 Formats R4 & R5

Those response formats are reserved for I/O mode (refer to the "SDIO Card Specification").

7.3.2.6 Format R7

This response token is sent by the card when a SEND_IF_COND command (CMD8) is received. The response length is 5 bytes. The structure of the first (MSB) byte is identical to response type R1. The other four bytes contain the card operating voltage information and echo back of check pattern in argument and are specified by the same definition as R7 response in SD mode. (Refer to Section 4.9).

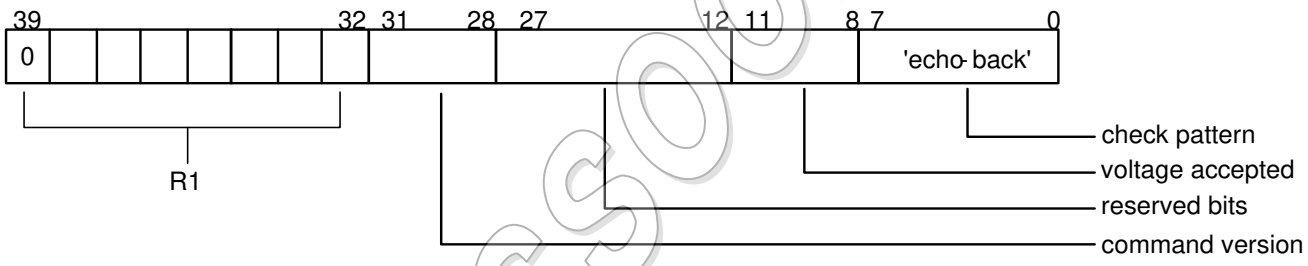

Figure 7-12 : R7 Response Format

7.3.3 Control Tokens

Data block transfer is controlled by some tokens.

7.3.3.1 Data Response Token

Every data block written to the card will be acknowledged by a data response token. It is one byte long and has the following format:

7	6	5	4	3	2	1	0
x	x	x	0	Status			1

The meaning of the status bits is defined as follows:

'010' - Data accepted.
'101' - Data rejected due to a CRC error.
'110' - Data Rejected due to a Write Error

In case of any error (CRC or Write Error) during Write Multiple Block operation, the host shall stop the data transmission using CMD12. In case of a Write Error (response '110'), the host may send CMD13 (SEND_STATUS) in order to get the cause of the write problem. ACMD22 can be used to find the number of well written write blocks.

7.3.3.2 Start Block Tokens and Stop Tran Token

Read and write commands have data transfers associated with them. Data is being transmitted or received via data tokens. All data bytes are transmitted MSB first.
Data tokens are 4 to 515 bytes long and have the following format:
For Single Block Read, Single Block Write and Multiple Block Read:

- First byte: Start Block

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	0

- Bytes 2-513 (depends on the data block length): User data
- Last two bytes: 16 bit CRC.

For Multiple Block Write operation:

- First byte of each block:
  If data is to be transferred then - Start Block Token

7	6	5	4	3	2	1	0
1	1	1	1	1	1	0	0

  If Stop transmission is requested - Stop Tran Token

7	6	5	4	3	2	1	0
1	1	1	1	1	1	0	1

Note that this format is used only for Multiple Block Write. In case of a Multiple Block Read the stop transmission is performed using STOP_TRAN Command (CMD12).

7.3.3.3 Data Error Token

If a read operation fails and the card cannot provide the required data, it will send a data error token instead. This token is one byte long and has the following format:

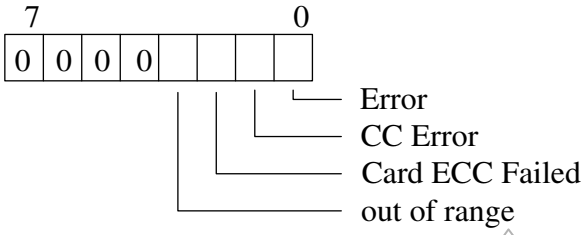

Figure 7-13 : Data Error Token

The 4 least significant bits (LSB) are the same error bits as in response format R2.

7.3.4 Clearing Status Bits

As described in the previous paragraphs, in SPI mode, status bits are reported to the host in three different formats: response R1, response R2, and data error token (the same bits may exist in multiple response types - e.g. Card ECC failed)

As in the SD mode, error bits are cleared when read by the host, regardless of the response format. State indicators are either cleared by reading or are cleared in accordance with the card state.

The following table summarizes the set and clear conditions for the various status bits:

Identifier	Included in resp	Type[1]	Value	Description	Clear Condition[2]
Out of range	R2 DataErr	E R X	'0'= no error '1'= error	The command argument was out of the allowed range for this card.	C
Address error	R1 R2	E R X	'0'= no error '1'= error	A misaligned address which did not match the block length was used in the command.	C
Erase sequence error	R1 R2	E R	'0'= no error '1'= error	An error in the sequence of erase commands occurred.	C
Erase param	R2	E X	'0'= no error '1'= error	An error in the parameters of the erase command sequence	C
Parameter error	R1 R2	E R X	'0'= no error '1'= error	An error in the parameters of the command	C
WP violation	R2	E R X	'0'= not protected '1'= protected	Attempt to program a write protected block.	C
Com CRC error	R1 R2	E R	'0'= no error '1'= error	The CRC check of the command failed.	C
Illegal command	R1 R2	E R	'0'= no error '1'= error	Command not legal for the card state	C
Card ECC failed	R2 DataEr	E X	'0'= success '1'= failure	Card internal ECC was applied but failed to correct the data.	C
CC error	R2 dataEr	E R X	'0'= no error '1'= error	Internal card controller error	C
Error	R2 dataEr	E R X	'0'= no error '1'= error	A general or an unknown error occurred during the operation.	C

Identifier	Included in resp	Type[1]	Value	Description	Clear Condition[2]
CSD_OVERWRITE	R2	E R X	'0'= no error '1'= error	Can be either of the following errors: - The read only section of the CSD does not match the card content. - An attempt to reverse the copy (set as original) or permanent WP (unprotected) bits was made.	C
WP erase skip	R2	S X	'0'= not protected '1'= protected	Only partial address space was erased due to existing write protected blocks.	C
Lock/Unlock cmd failed	R2	X	'0'= no error '1'= error	Sequence or password errors during card lock/unlock operation.	C
Card is locked	R2	S X	'0' = card is not locked '1' = card is locked	Card is locked by a user password.	A
Erase reset	R1 R2	S R	'0'= cleared '1'= set	An erase sequence was cleared before executing because an out of erase sequence command was received	C
In Idle state	R1 R2	S R	0 = Card is ready 1 = Card is in idle state	The card enters the idle state after power up or reset command. It will exit this state and become ready upon completion of its initialization procedures.	A

Table 7-6 : SPI Mode Status Bits

1) Type:
E: Error bit.
S: State bit.
R: Detected and set for the actual command response.
X: Detected and set during command execution. The host can get the status by issuing a command with R1 response.

2) Clear Condition:
A: According to the current state of the card.
C: Clear by read

7.4 Card Registers

In SPI mode, only the RCA register is not accessible. Formats of other registers are identical to the formats in the SD mode.

7.5 SPI Bus Timing Diagrams

This section is a blank in the Simplified Specification.

7.6 SPI Electrical Interface

The electrical interface is identical to SD mode with the exception of the programmable card output drivers' option, which is not supported in SPI mode.

7.7 SPI Bus Operating Conditions

Bus operating conditions are identical to SD mode

7.8 Bus Timing

Bus timing is identical to SD mode. The timing of the CS signal is the same as any other card input.

8. Sections Effective to SD I/F Mode and UHS-II Mode

This section is a blank in the Simplified Specification.

Appendix A (Normative) : Reference

A.1 Related Documentation

This section is a blank in the Simplified Specification.

Appendix B (Normative) : Special Terms

B.1 Terminology

active AU	The AU that is currently designated for Video Speed Class recording
assigned AUs	The AUs that have been assigned and not completely written
block	A number of bytes, basic data transfer unit
broadcast	A command sent to all cards on the SD bus
Blocklen	Block Length set by CMD16
Cache	A faster memory in card that may be volatile to store host data temporarily
DIR slot	Card supporting Video Speed Class has eight slots to register locations of DIR write to manage average time of FAT update.
Distributed	A signal path between host and card which has a distributed system effects. As described in transmission line theory.
Extension Register	Register defined by a Function Specification in Extension Register Space.
Extension Register Space	Register Spaces accessible by CMD48/49/58/59 with 17-bit ADDR and FNO. There are two types of spaces: memory space and I/O space.
Flash	A type of multiple time programmable non-volatile memory
File System Area	The area comprising Partition table, FAT, Bitmap, Directory Entry, etc.
Fixed Data Window	There is an overlapped area of valid data window for all delay variation.
group	A number of sectors, composite erase and write protect unit
LBA	A Logical Block Address identifies a specific sector
Logical Erase	Erasing the logical address to physical address mapping
Lumped	A signal path between host and card which is considerably small compared to the signal rise time. It is considered as "lumped" system
open-drain	A logical interface operation mode. An external resistor or current source is used to pull the interface level to HIGH, the internal transistor pushes it to LOW
payload	Net data
push-pull	A logical interface operation mode, a complementary pair of transistors is used to push the interface level to HIGH or LOW
sector	A number of blocks, basic erase unit
Sequential CQ mode	Command Queue mode where tasks are submitted and executed in increasing order of task ID from Task 0
Self Maintenance	A method where internal operations are carried out based on Host's enablement
Speed Class	Minimum performance defined in Default and High Speed Modes
Speed Grade	Minimum performance defined in UHS-I and UHS-II mode
stuff bit	Filling bits to ensure fixed length frames for commands and responses
suspended AU	An AU that has been addressed by a CMD20 "Suspend AU" command
three-state driver	A driver stage which has three output driver states: HIGH, LOW and high impedance (which means that the interface does not have any influence on the interface level)
token	Code word representing a command
Tuning	Host adjusts sampling clock by Send Tuning Block Command.
Variable Data Window	An overlapped area of valid data window is not available or too small for all Process, Voltage and Temperature variations.
Video Speed Class	Minimum performance independently defined from Speed Class and Speed Grade
Voluntary CQ mode	Command Queue mode where tasks are submitted in arbitrary order and executed based on ready state indicated by card

B.2 Abbreviations

ACMD6	Set bus width command
ACMD41	Initialization command
AU	Allocation Unit
CID	Card IDentification number register
CLK	clock signal
CMD	command line or SD bus command (if extended CMDXX)
CRC	Cyclic Redundancy Check
CSD	Card Specific Data register
CMD0	Reset command
CMD8	Voltage check command
CMD6	Switch command used for selecting one of UHS-I modes
CMD11	Voltage switch command to change signaling level 3.3V to 1.8V.
CMD19	A new command for sending tuning block
COP	Card Ownership Protection
CQ	Command Queue
DAT or DAT[3:0]	4-bit data line of SD bus
DDR	Double data rate signaling
DDR50	One of UHS modes with double data rate. Up to 50MB/sec at 50MHz
DS	Default Speed Mode
DSR	Driver Stage Register
ECC	Error Correction Code
eSD	Embedded SD Memory Device defined by Part 1 eSD Addendum
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FD156	UHS-II Full Duplex mode with data transfer rate up to 156MB/s
FD312	UHS-II Full Duplex mode with data transfer rate up to 312MB/s
FD624	UHS-II Full Duplex mode with data transfer rate up to 624MB/s
FEP	Force Erase Password
HD312	UHS-II Half Duplex with 2 Lanes mode with data transfer rate up to 312MB/s
Host-SDR-FD	One of host types with SDR signaling, fixed-delay (can't use tuning)
Host-SDR-VD	One of host types with SDR signaling, variable-delay (can use tuning)
Host-DDR	One of host types with DDR signaling
HS	High Speed Mode
IOPS	Input/Output Operations Per Second
LOW, HIGH	Binary interface states with defined assignment to a voltage level
LV50	One of LV card classification type that supports single data rate up to 50MB/sec at 100MHz
LV104	One of LV card classification type that supports single data rate up to 104MB/sec at 208MHz
LV156	One of LV card classification type that supports UHS-II Full Duplex mode with data transfer rate up to 156MB/s. May support Half Duplex mode with data transfer rate up to 312MB/s.
LV624	One of LV card classification type that supports UHS-II Full Duplex mode with data transfer rate up to 624MB/s. May support Half Duplex mode with data transfer rate up to 312MB/s.
MSB, LSB	The Most Significant Bit or Least Significant Bit
MLCC	Multi-Layer Ceramic Capacitor
MTP	Multiple Time Programmable memory
N_{ERASE}	The recommended numbers of AUs to be erased in one erase operation.
T_{ERASE}	Timeout value used for erasing multiple AU's as specified by ERASE_SIZE.

T_{OFFSET}	Offset time used for calculating erase timeout.
NSAC	Defines the worst case for the clock rate dependent factor of the data access time
OCR	Operation Conditions Register
OTP	One Time Programmable memory
P_w	Performance of Write
P_m	Performance of Move
P_r	Performance of Read
PDN	Power Delivery Network
PRw	Performance of Random Write
PRr	Performance of Random Read
PSSw	Performance of Sustained Sequential Write
RCA	Relative Card Address register
ROM	Read Only Memory
RU	Recording Unit
SDCLK	Clock line of SD bus
S18R	Switching to 1.8V Request in ACMD41 argument
S18A	Switching to 1.8V Accepted in ACMD41 response
SPI	Serial Peripheral Interface
SU	Sub Unit
TAAC	Defines the time dependent factor of the data access time
tag	Marker used to select groups or sector to erase
TBD	To Be Determined (in the future)
T_{fw}	FAT write time
T_{fr}	FAT read time
t_{ODLY}	Output Delay from SDCLK under all delay parameters condition.
UHS	Ultra High Speed
UI	Unit Interval is one bit nominal time, SDCLK nominal period.
SD Bus I/F	Interface using contact pin numbers 1 to 9.
SDR	Single data rate signaling
SDR12	One of UHS-I modes with single data rate. Up to 12.5MB/sec at 25MHz
SDR25	One of UHS-I modes with single data rate. Up to 25MB/sec at 50MHz
SDR50	One of UHS-I modes with single data rate. Up to 50MB/sec at 100MHz
SDR104	One of UHS-I modes with single data rate. Up to 104MB/sec at 208MHz
UHS50	One of UHS-I Card Types supporting SDR50
UHS104	One of UHS-I Card Types supporting SDR104
UHS156	UHS-II Generation 1 Card Type supporting FD156 and HD312 (Optional)
UHS624	UHS-II Generation 2 Card Type supporting FD624
UHS-II I/F	Interface using contact pin numbers 7 to 8 and 10 to 17.
VCA	Card accepted voltage range
VHS	Host supplied voltage range
V_{DD}	+ power supply of non UHS-II Card
V_{DD1}	3.3V range power supply for UHS-II Card (First row)
V_{DD2}	1.8V range power supply for UHS-II Card (Second row)
VSC	Video Speed Class
V_{SS}	Power supply ground
X5R/X7R	Symbol for dielectric material of capacitors

Appendix C (Informative) : Examples for Fixed Delay UHS-I Host Design

This section is a blank in the Simplified Specification.

Appendix D : UHS-I Tuning Procedure

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Appendix E : Host Power Delivery Network (PDN) Design Guide

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Appendix F : Application Notes of Extension Function

F.1 Identification of Function Driver

There are two types of function drivers. "Standard Driver" controls a Standard Function, which will be defined by a Function Specification and it will be provided by OS or Host System vendor. "Particular Driver" controls a Particular Function and it will be provided by the function developer.

During a function initialization, Host Driver finds and loads a most suitable function driver installed on Host System referring to 4 codes in the General Information.

SFC (Standard Function Code) 2 byte
FCC (Function Capability Code) 2 byte
FMC (Function Manufacturer Code) 2 byte
PFC (Particular Function Code) 2 byte

Standard Driver is selected by SFC and FCC. SFC>0 and FCC=0 means that there is a unique function driver for a SFC and Host Driver finds the driver by only SFC. SFC>0 and FCC>0 means that there are multiple of function drivers to a SFC. These Card Drivers will be installed to Host System with "Capability Information" which corresponds to FCC. Host Driver selects one driver of which Capability Information accords with FCC. SFC=0 means that there is no Standard Driver and then Host Driver finds a Particular Driver which accords with FMC and PFC.
Table F - 1 shows combination of the codes to identify a function driver. If SFC>0, FMC>0 and PFC>0, the function may use Standard Driver and Particular Driver depends on driver installation to Host System. Use of Particular Driver is higher priority for supporting higher functionality than use of Standard Driver

SFC	FCC	FMC	PFC	Selection of Function Driver
Non-zero	0000h	0000h	0000h	Select a Standard Driver by only SFC
Non-zero	Non-zero	0000h	0000h	Host selects one of Drivers by FCC
0000h	0000h	Non-zero	Non-zero	Select Particular Function Driver by FMC and PFC
Non-zero	any value	Non-zero	Non-zero	Select either Particular or Standard Function Driver Particular Driver has higher priority

Table F - 1 : Combination of Codes to Identify a Function Driver

F.2 Concept of Event Detection Method

To use Event Indication Method is defined in Section 5.7.5, host support is required for event detection and function driver management. Host Controller or Host Driver detects FX_EVENT generation and then interrupt hander calls a Function Driver to deal with the event.

F.2.1 Role of Driver Modules

Figure F - 1 shows an example configuration of hardware and drivers layers. Some of functions may generate events.

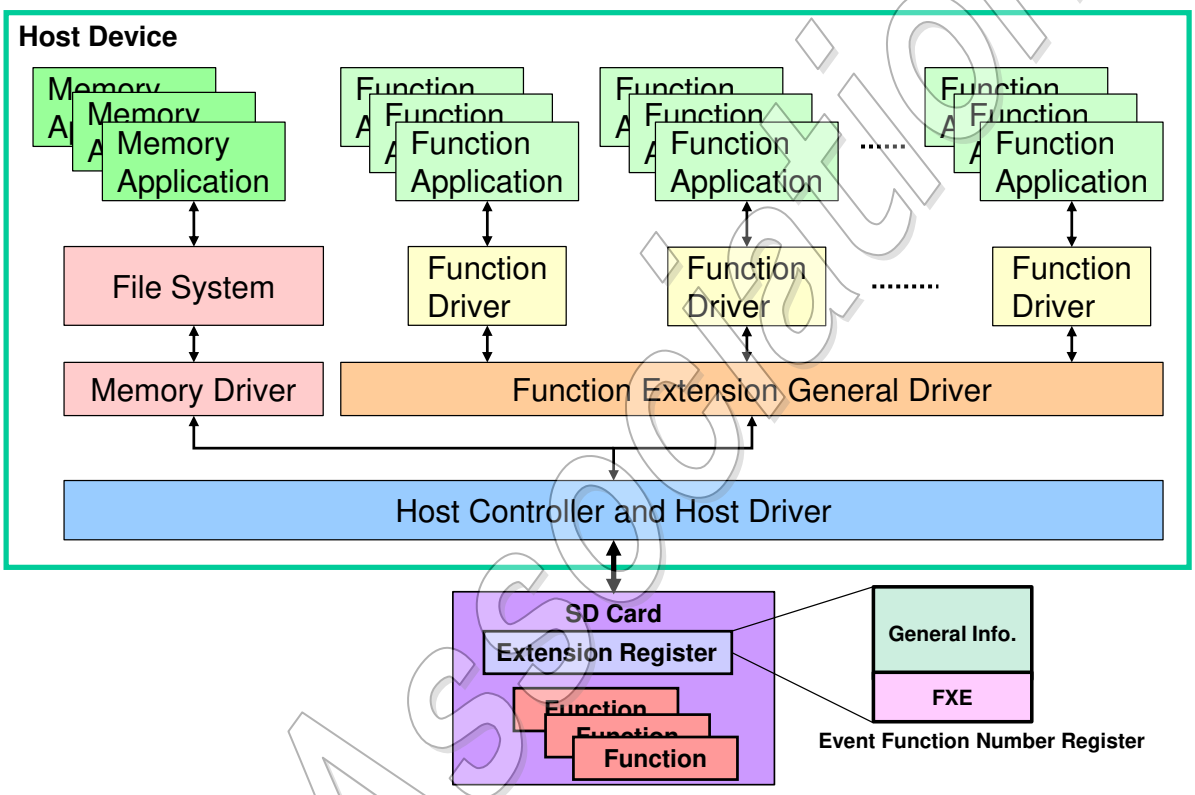

Figure F - 1 : Hardware and Driver Layer of Host and Card

- **Host Controller and Host Driver**
  Host Controller is an interface device between Host System (System Memory) and SD Card that is connected to system bus. Host Driver is software for controlling the Host Controller. Host Driver manages to issue SD Commands to SD Card according to requests from Memory Driver and Function Drivers by accessing Host Controller Registers. Host Controller has capability to generate interrupt to host CPU according to the response of the SD Card. FX_EVENT on R1 is one of interrupt events by Function Devices. On detecting FX_EVENT, Host Driver gets "Function Extesion General Driver" to deal with the event.
- **Memory Driver**
  SD Memory Card Driver to manage memory access to or from SD Memory Card. Indication of FX_EVENT is not supported by this driver.
- **Function Driver**
  This driver knows how to control a function and generates commands sequece to control Extesion Registers according to requests of application. This driver knows how to deal with the evets of the function. Funciton Driver will be provided by card vendor.
- **Function Extesion General Driver (FEGD)**

During SD Card initialization, this driver finds and loads a Function Driver installed on Host System for controlling a function which is supported by the SD Card. This driver manages communication between multiple of Function Drivers and Host Driver. On detecting FX_EVENT informed by Host Driver, this driver reads FXE Register Set and determines which Function Driver to deal with the event.

F.2.2 Host Implementation to use Event Detection Method

- **Card Initialization**
  When Host Controller detects SD Card, Host Driver will initialize memory portion at first. By detecting Extension Function support on the card, Host Driver tries to find and load Function Drivers installed in the Host System by referring to the General Information. If a Function Driver can be loaded, it is connected to "Function Extension General Driver", which can communicate multiple of function drivers. Host Driver is connected to the "Function Extension General Driver". Standard Driver Interface is assumed to communicate between two driver layers.

- **Event Detection**
  While Host Controller issues SD Commands to the card, host may check event generation by R1 response of any command without issuing extra-commands for polling. While there is no command to be issued to the card, Host Driver inserts CMD13 for polling events at some interval.
  By reading FXE Register Set, Function Extension General Driver determines priority of event handling and get a Function Driver to deal with the event.